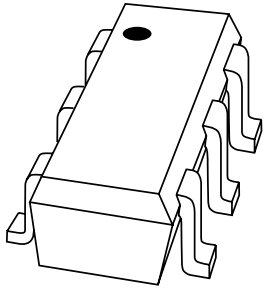


# DATA SHEET



## **BF1206** Dual N-channel dual-gate MOS-FET

Product specification

2003 Nov 17

# Dual N-channel dual-gate MOS-FET

# BF1206

### FEATURES

- Two low noise gain controlled amplifiers in a single package
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

### APPLICATIONS

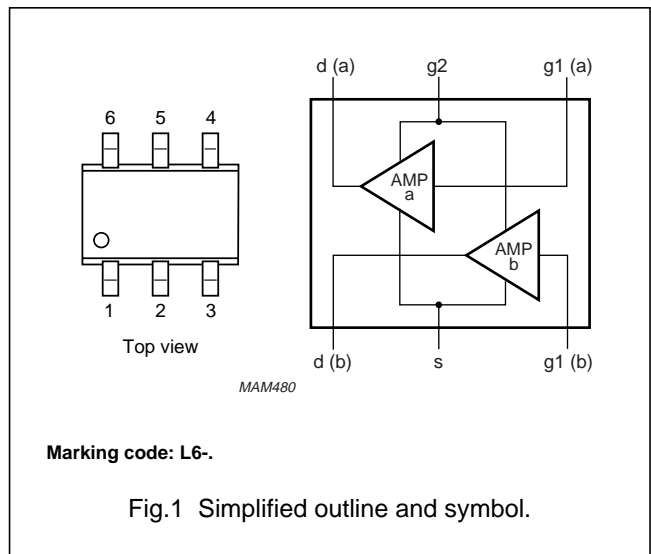
- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage, such as digital and analog television tuners.

### DESCRIPTION

The BF1206 is a combination of two different dual gate MOS-FET amplifiers with shared source and gate 2 leads. The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor is encapsulated in SOT363 micro-miniature plastic package.

### PINNING - SOT363

PIN	DESCRIPTION
1	drain (b)
2	source
3	gate 1 (b)
4	gate 1 (a)
5	gate 2
6	drain (a)



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per MOS-FET; unless otherwise specified</b>						
$V_{DS}$	drain-source voltage		–	–	6	V
$I_D$	drain current (DC)		–	–	30	mA
$ y_{fs} $	forward transfer admittance	amp. a: $I_D = 18$ mA	33	38	48	mS
		amp. b: $I_D = 12$ mA	29	34	44	mS
$C_{ig1-s}$	input capacitance at gate 1	amp. a: $I_D = 18$ mA; $f = 1$ MHz	–	2.4	2.9	pF
		amp. b: $I_D = 12$ mA; $f = 1$ MHz	–	1.7	2.2	pF
$C_{rss}$	reverse transfer capacitance	$f = 1$ MHz	–	15	–	fF
$X_{mod}$	cross-modulation	amp. a: input level for $k = 1\%$ at 40 dB AGC	102	105	–	dB $\mu$ V
		amp. b: input level for $k = 1\%$ at 40 dB AGC	100	103	–	dB $\mu$ V
NF	noise figure	amp. a: $f = 400$ MHz; $I_D = 18$ mA	–	1.3	1.9	dB
		amp. b: $f = 800$ MHz; $I_D = 12$ mA	–	1.4	2.0	dB
		amp. a: $f = 11$ MHz; $I_D = 18$ mA	–	3	–	dB
		amp. b: $f = 11$ MHz; $I_D = 12$ mA	–	3.5	–	dB

## Dual N-channel dual-gate MOS-FET

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**CAUTION**

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BF1206	–	plastic surface mounted package; 6 leads	SOT363

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per MOS-FET; unless otherwise specified</b>					
$V_{DS}$	drain-source voltage		–	6	V
$I_D$	drain current (DC)		–	30	mA
$I_{G1}$	gate 1 current		–	$\pm 10$	mA
$I_{G2}$	gate 2 current		–	$\pm 10$	mA
$P_{tot}$	total power dissipation	$T_s \leq 107\text{ °C}$ ; note 1	–	180	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C

**Note**

- $T_s$  is the temperature at the soldering point of the source lead.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	240	K/W

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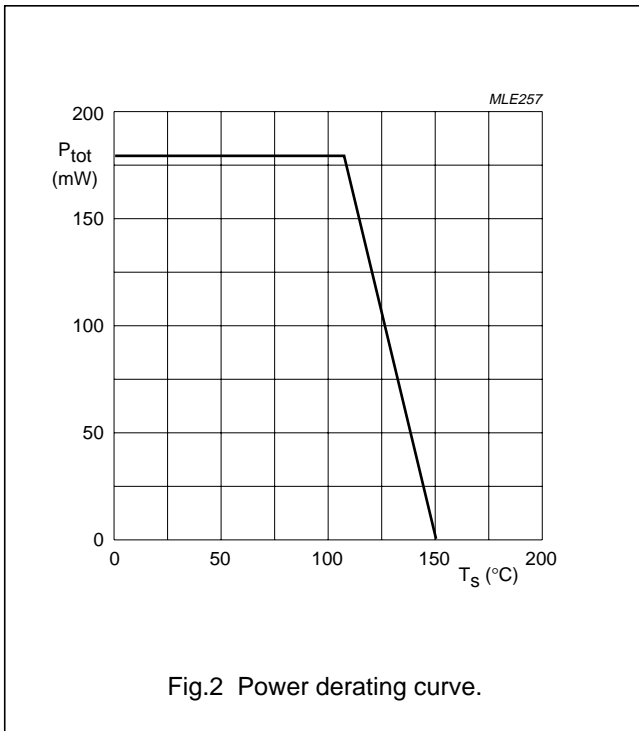


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T<sub>j</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per MOS-FET unless otherwise specified</b>					
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>G1-S</sub> = V <sub>G2-S</sub> = 0; I <sub>D</sub> = 10 μA	6	–	V
V <sub>(BR)G1-SS</sub>	gate-source breakdown voltage	V <sub>GS</sub> = V <sub>DS</sub> = 0; I <sub>G1-S</sub> = 10 mA	6	10	V
V <sub>(BR)G2-SS</sub>	gate-source breakdown voltage	V <sub>GS</sub> = V <sub>DS</sub> = 0; I <sub>G2-S</sub> = 10 mA	6	10	V
V <sub>(F)S-G1</sub>	forward source-gate voltage	V <sub>G2-S</sub> = V <sub>DS</sub> = 0; I <sub>S-G1</sub> = 10 mA	0.5	1.5	V
V <sub>(F)S-G2</sub>	forward source-gate voltage	V <sub>G1-S</sub> = V <sub>DS</sub> = 0; I <sub>S-G2</sub> = 10 mA	0.5	1.5	V
V <sub>G1-S(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 5 V; V <sub>G2-S</sub> = 4 V; I <sub>D</sub> = 100 μA	0.3	1	V
V <sub>G2-S(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 5 V; V <sub>G1-S</sub> = 5 V; I <sub>D</sub> = 100 μA	0.35	1	V
I <sub>DSX</sub>	drain-source current	amp. a: V <sub>G2-S</sub> = 4 V; V <sub>DS</sub> = 5 V; R <sub>G</sub> = 91 kΩ; note 1	14	23	mA
		amp. b: V <sub>G2-S</sub> = 4 V; V <sub>DS</sub> = 5 V; R <sub>G</sub> = 150 kΩ; note 1	9	17	mA
I <sub>G1-S</sub>	gate cut-off current	V <sub>G1-S</sub> = 5 V; V <sub>G2-S</sub> = V <sub>DS</sub> = 0	–	50	nA
I <sub>G2-S</sub>	gate cut-off current	V <sub>G2-S</sub> = 5 V; V <sub>G1-S</sub> = V <sub>DS</sub> = 0	–	20	nA

Note

1. R<sub>G1</sub> connects gate 1 to V<sub>GG</sub> = 5 V.

## Dual N-channel dual-gate MOS-FET

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**DYNAMIC CHARACTERISTICS AMPLIFIER a**Common source;  $T_{amb} = 25\text{ °C}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $V_{DS} = 5\text{ V}$ ;  $I_D = 18\text{ mA}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	33	38	48	mS
$C_{ig1-ss}$	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.4	2.9	pF
$C_{ig2-ss}$	input capacitance at gate 2	$f = 1\text{ MHz}$	–	3.2	–	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz}$	–	1.1	–	pF
$C_{rss}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
NF	noise figure	$f = 11\text{ MHz}$ ; $G_S = 20\text{ mS}$ ; $B_S = 0$	–	3	–	dB
		$f = 400\text{ MHz}$ ; $Y_S = Y_{S\text{ opt}}$	–	1.3	1.9	dB
		$f = 800\text{ MHz}$ ; $Y_S = Y_{S\text{ opt}}$	–	1.6	2.2	dB
$G_{tr}$	power gain	$f = 200\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{S\text{ opt}}$ ; $G_L = 0.5\text{ mS}$ ; $B_L = B_{L\text{ opt}}$ ; note 1	–	35	–	dB
		$f = 400\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{S\text{ opt}}$ ; $G_L = 1\text{ mS}$ ; $B_L = B_{L\text{ opt}}$ ; note 1	–	30	–	dB
		$f = 800\text{ MHz}$ ; $G_S = 3.3\text{ mS}$ ; $B_S = B_{S\text{ opt}}$ ; $G_L = 1\text{ mS}$ ; $B_L = B_{L\text{ opt}}$ ; note 1	–	23	–	dB
$X_{mod}$	cross-modulation	input level for $k = 1\%$ ; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 2				
		at 0 dB AGC	90	–	–	dB $\mu$ V
		at 10 dB AGC	–	92	–	dB $\mu$ V
	at 40 dB AGC	102	105	–	dB $\mu$ V	

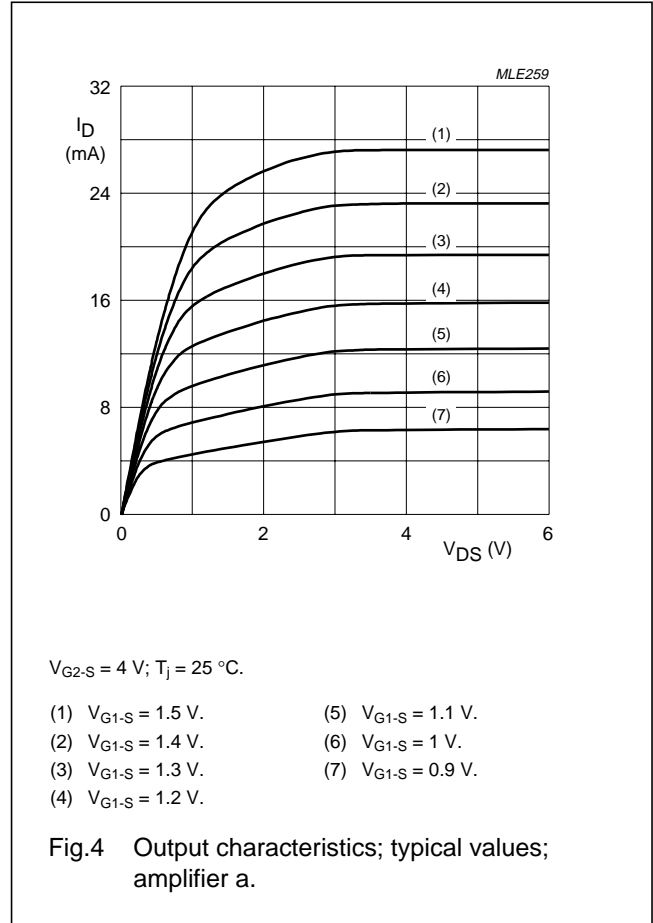
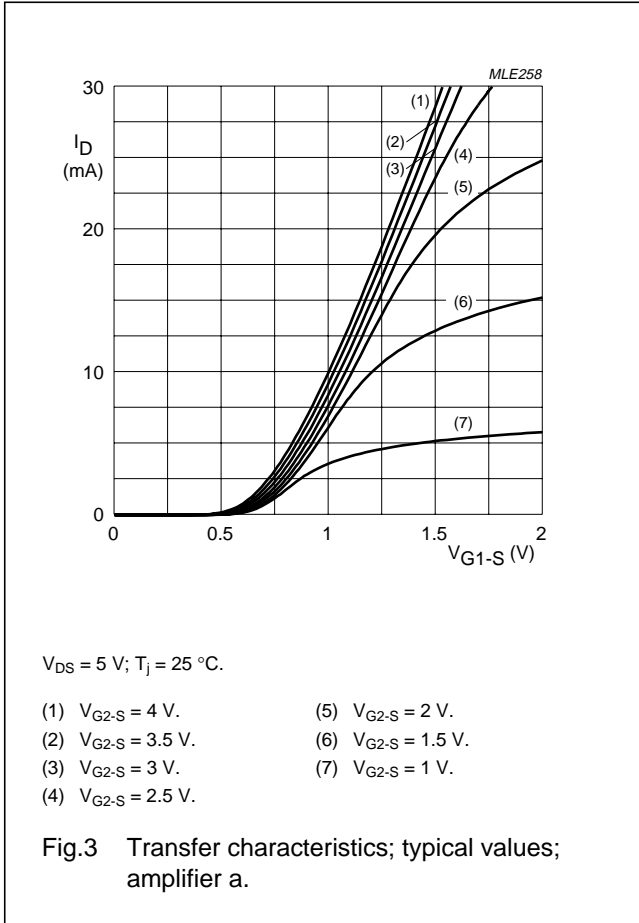
**Notes**

1. Calculated from measured s-parameters.
2. Measured in Fig.35 test circuit.

Dual N-channel dual-gate MOS-FET

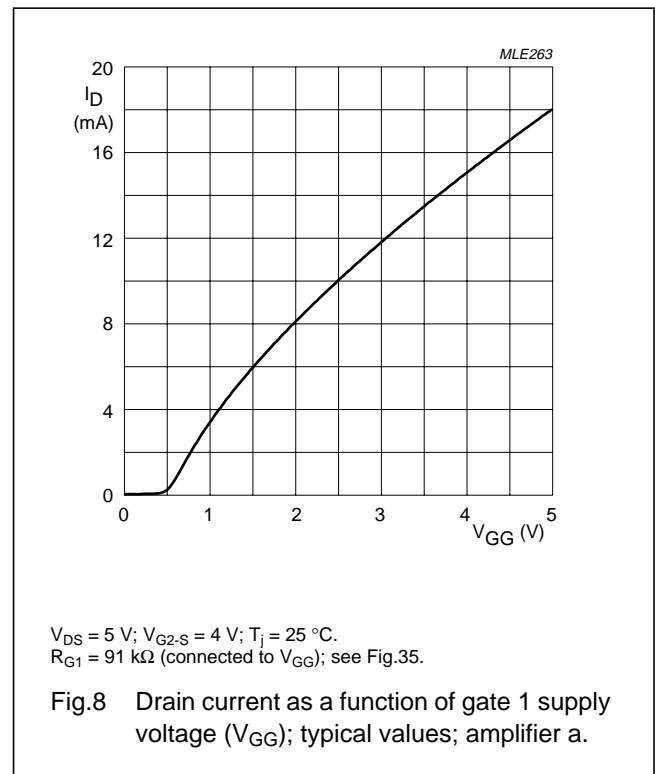
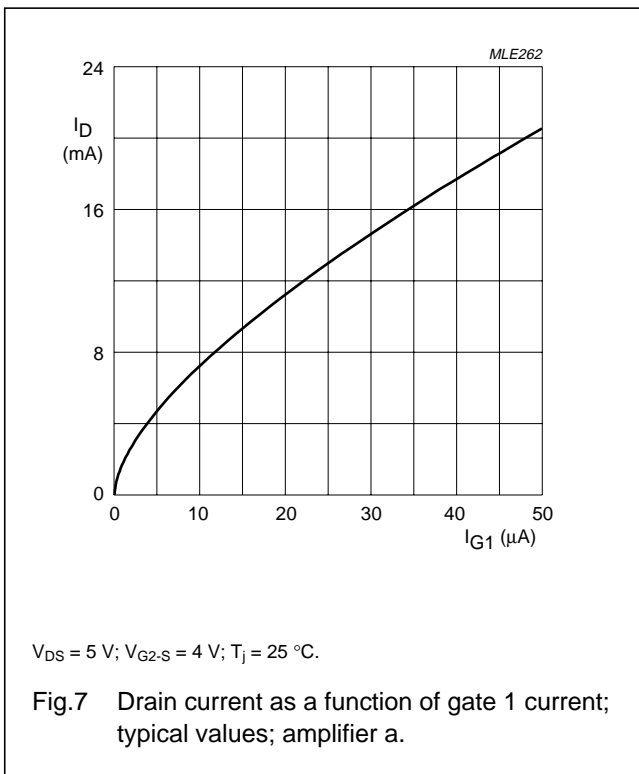
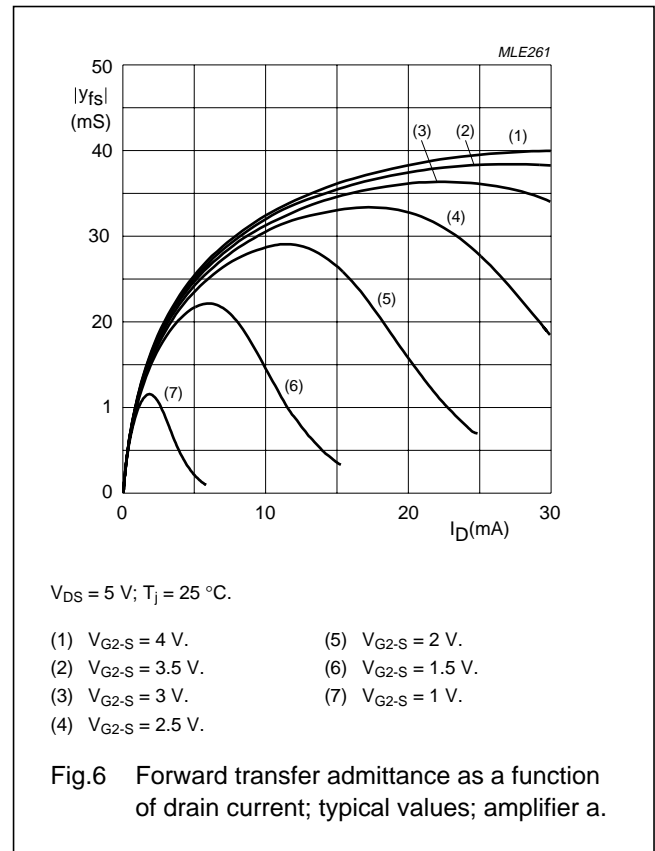
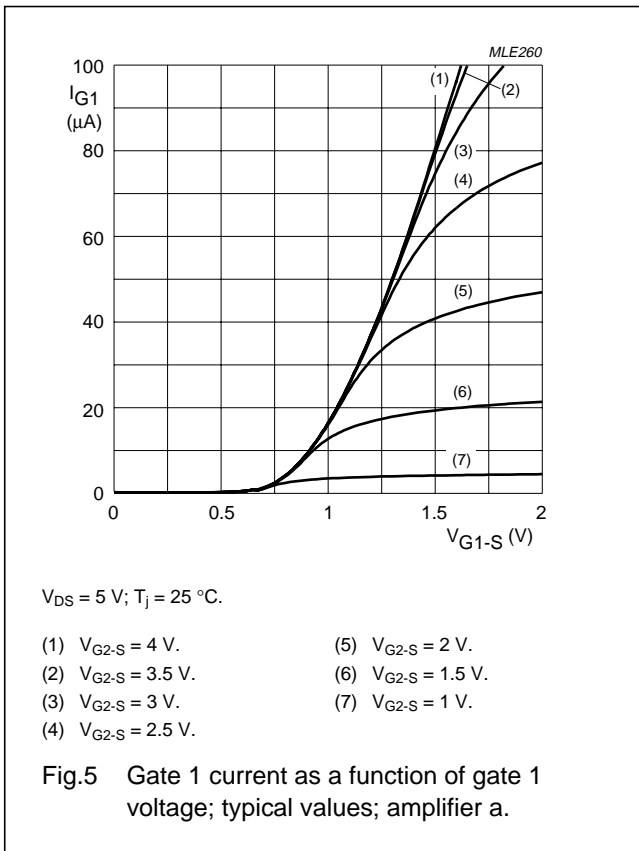
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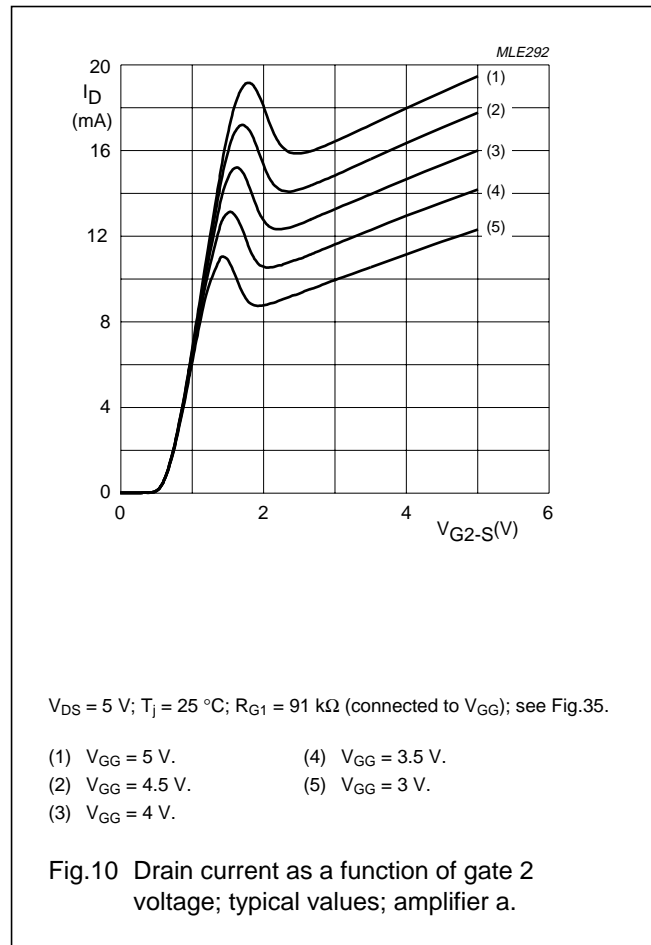
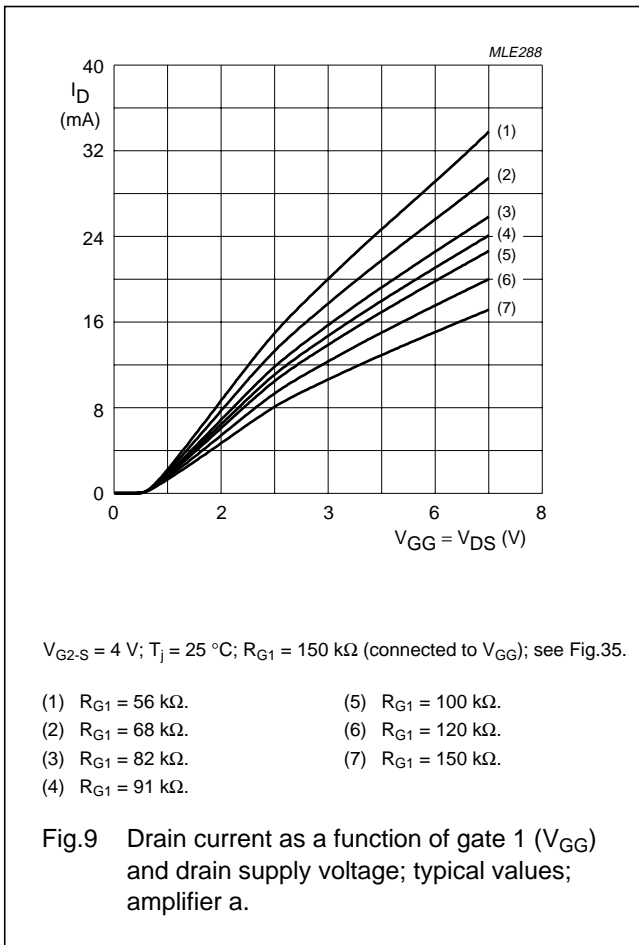
Dual N-channel dual-gate MOS-FET

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Dual N-channel dual-gate MOS-FET

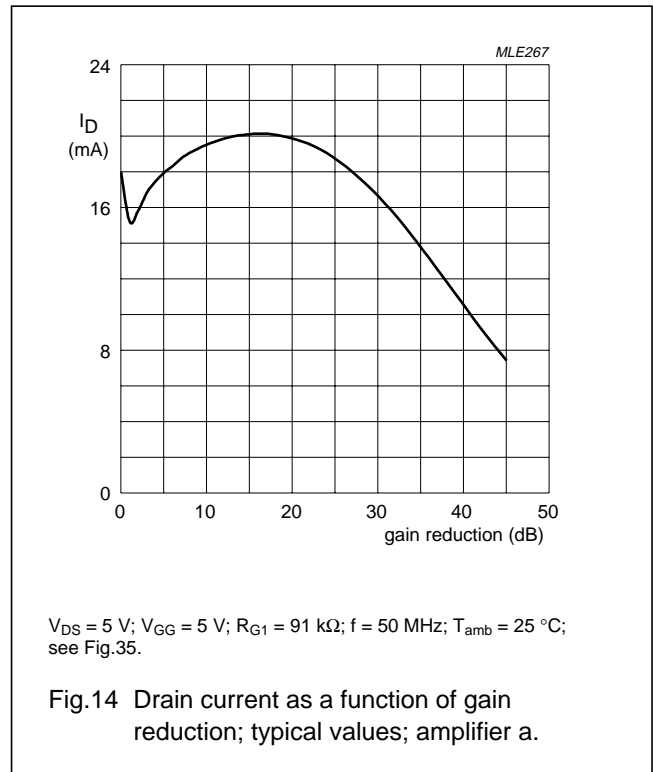
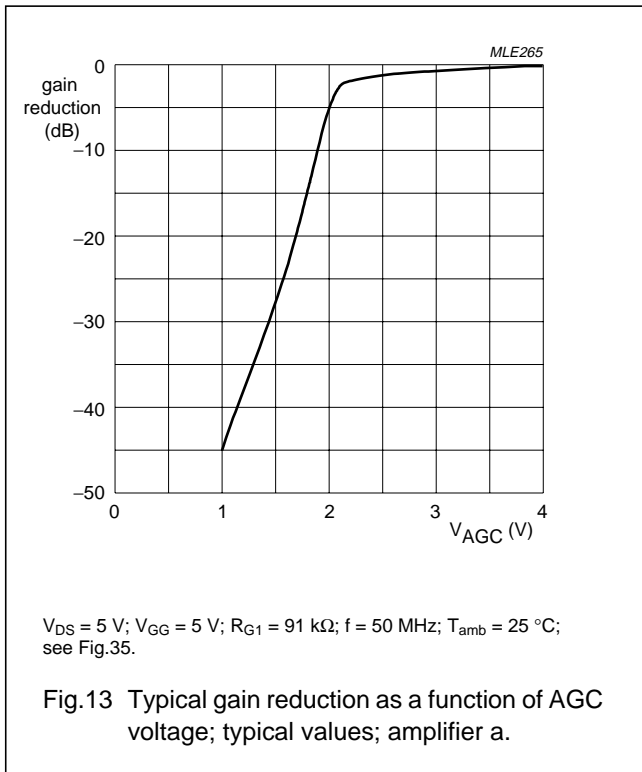
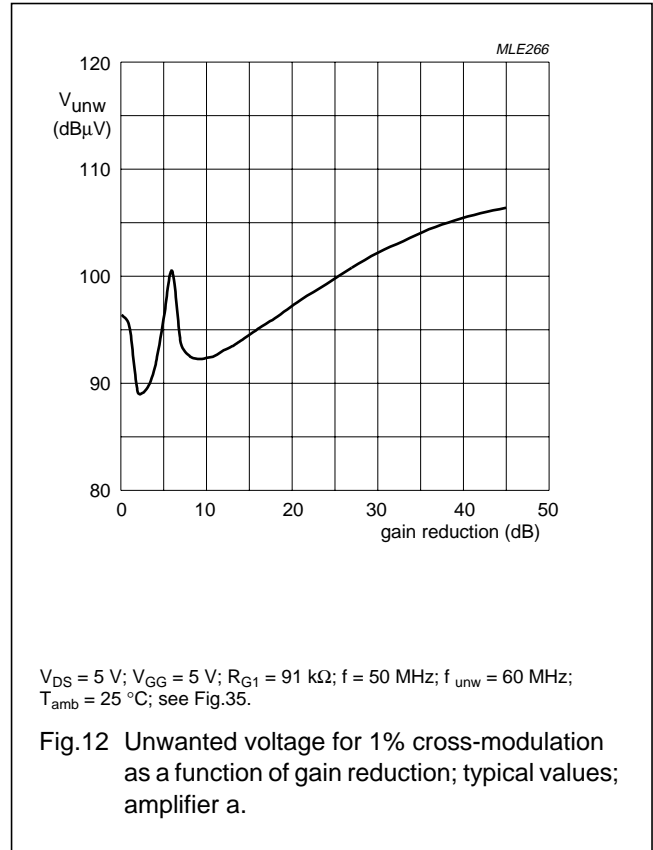
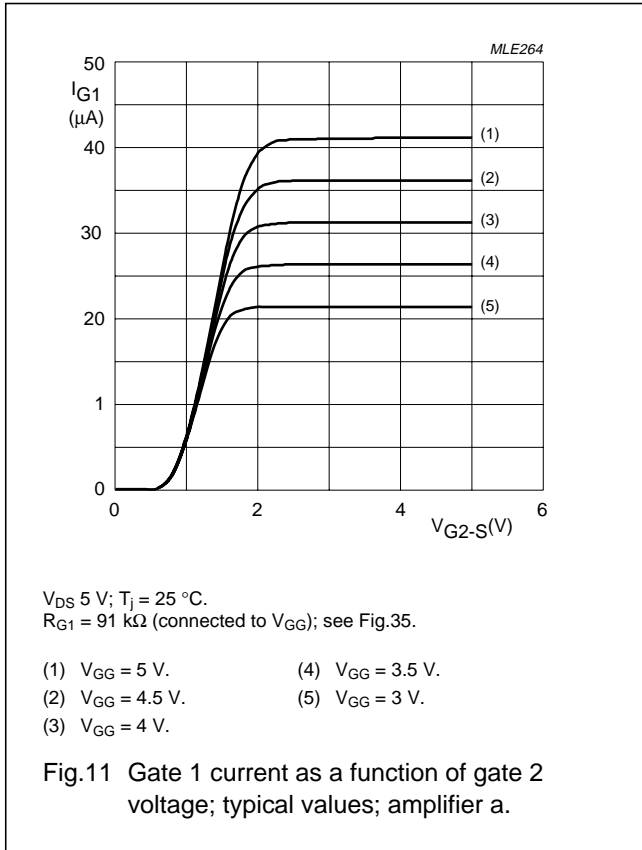
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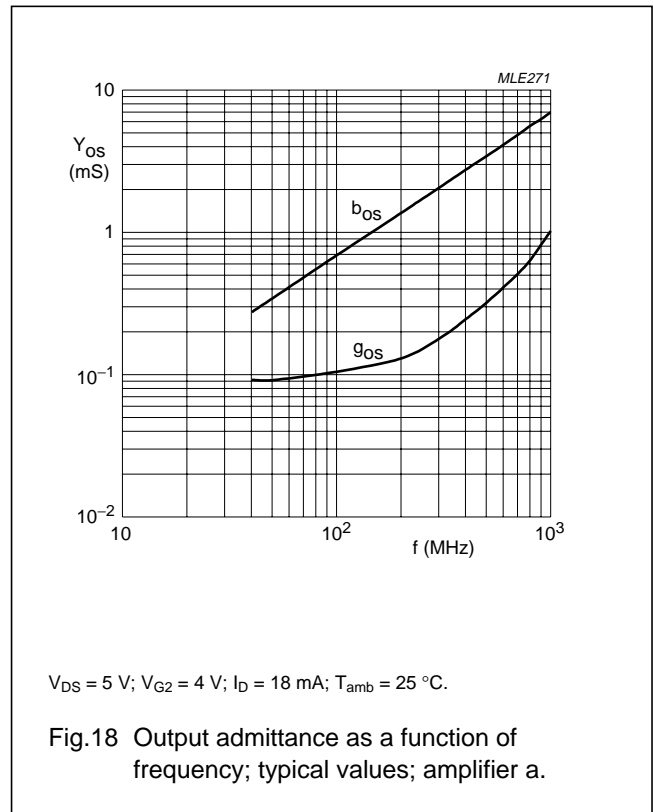
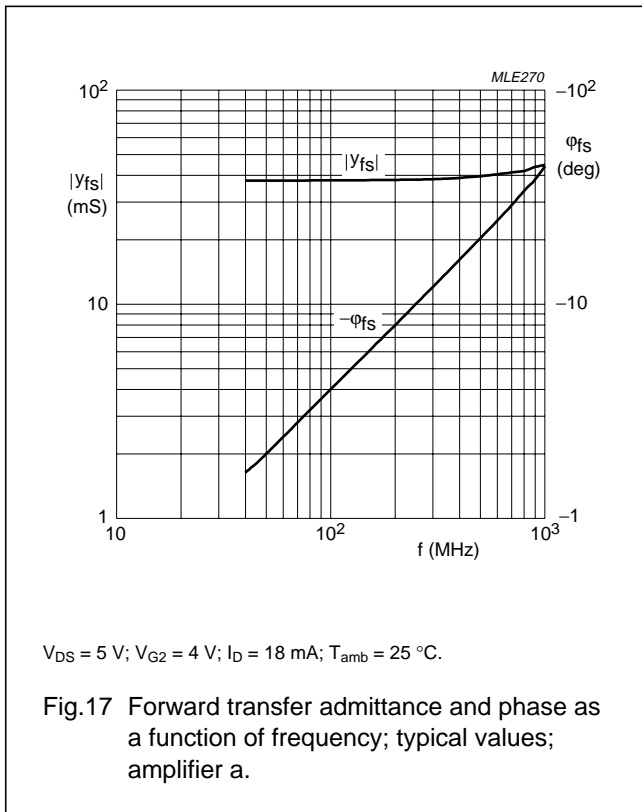
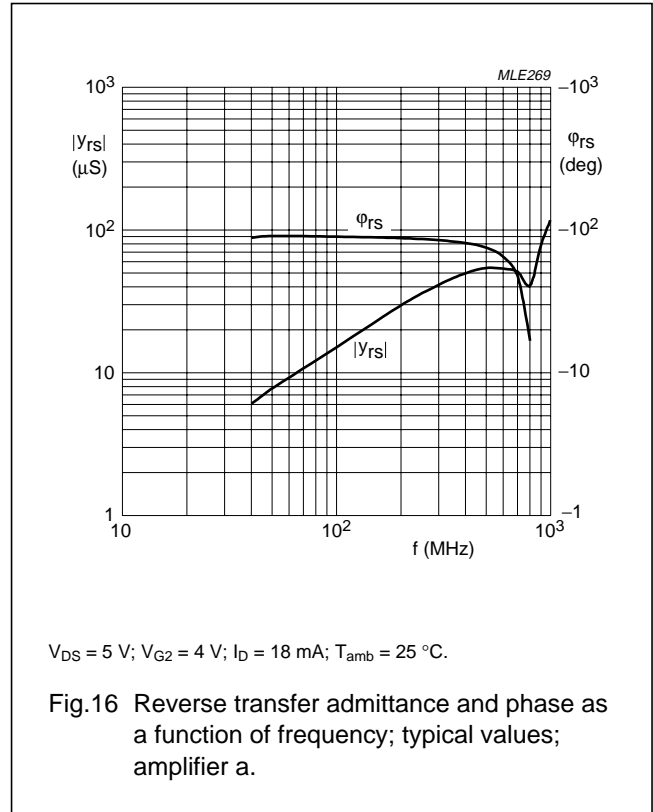
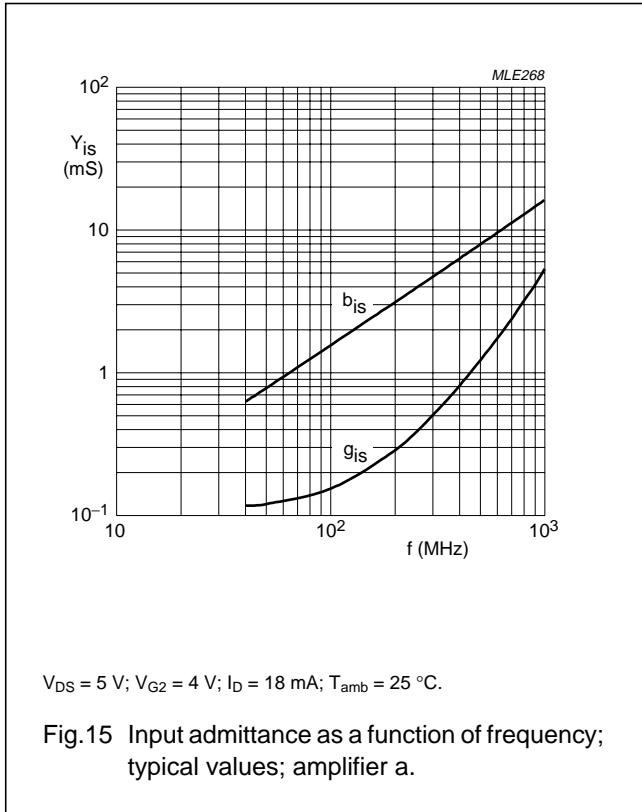
Dual N-channel dual-gate MOS-FET

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Dual N-channel dual-gate MOS-FET

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## Dual N-channel dual-gate MOS-FET

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**Amplifier a scattering parameters** $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 18\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$ 

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.988	-4.62	3.72	174.72	0.0008	86.73	0.991	-2.07
100	0.984	-9.23	3.71	169.42	0.0015	84.39	0.989	-4.16
200	0.971	-18.33	3.66	159.05	0.0029	79.96	0.986	-8.24
300	0.951	-27.32	3.58	148.77	0.0038	76.62	0.980	-12.32
400	0.926	-36.04	3.47	138.74	0.0044	74.42	0.973	-16.33
500	0.896	-44.50	3.36	129.05	0.0046	74.84	0.965	-20.25
600	0.865	-52.63	3.23	119.67	0.0043	79.73	0.958	-24.20
700	0.832	-60.47	3.09	110.43	0.0038	92.63	0.951	-28.14
800	0.797	-67.66	2.91	101.40	0.0028	118.47	0.937	-32.14
900	0.769	-75.01	2.83	93.09	0.0051	146.61	0.940	-35.76
1000	0.732	-81.73	2.67	84.05	0.0071	159.78	0.937	-39.86

**Noise data** $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 18\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$ 

f (MHz)	F <sub>min</sub> (dB)	Γ <sub>opt</sub>		R <sub>n</sub> (Ω)
		(ratio)	(deg)	
400	1.3	0.618	22.7	26.7
800	1.6	0.593	44.1	29.7

## Dual N-channel dual-gate MOS-FET

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**DYNAMIC CHARACTERISTICS AMPLIFIER b**Common source;  $T_{amb} = 25\text{ °C}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $V_{DS} = 5\text{ V}$ ;  $I_D = 12\text{ mA}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	29	34	44	mS
$C_{ig1-ss}$	input capacitance at gate 1	$f = 1\text{ MHz}$	–	1.7	2.2	pF
$C_{ig2-ss}$	input capacitance at gate 2	$f = 1\text{ MHz}$	–	4.2	–	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz}$	–	0.85	–	pF
$C_{rss}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
F	noise figure	$f = 11\text{ MHz}$ ; $G_S = 20\text{ mS}$ ; $B_S = 0$	–	3.5	–	dB
		$f = 400\text{ MHz}$ ; $Y_S = Y_{S\text{ opt}}$	–	1.3	1.9	dB
		$f = 800\text{ MHz}$ ; $Y_S = Y_{S\text{ opt}}$	–	1.4	2	dB
$G_{tr}$	power gain	$f = 200\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{S\text{ opt}}$ ; $G_L = 0.5\text{ mS}$ ; $B_L = B_{L\text{ opt}}$ ; note 1	–	35	–	dB
		$f = 400\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{S\text{ opt}}$ ; $G_L = 1\text{ mS}$ ; $B_L = B_{L\text{ opt}}$ ; note 1	–	31	–	dB
		$f = 800\text{ MHz}$ ; $G_S = 3.3\text{ mS}$ ; $B_S = B_{S\text{ opt}}$ ; $G_L = 1\text{ mS}$ ; $B_L = B_{L\text{ opt}}$ ; note 1	–	27	–	dB
$X_{mod}$	cross-modulation	input level for $k = 1\%$ ; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 2				
		at 0 dB AGC	90	–	–	dB $\mu$ V
		at 10 dB AGC	–	90	–	dB $\mu$ V
		at 40 dB AGC	100	103	–	dB $\mu$ V

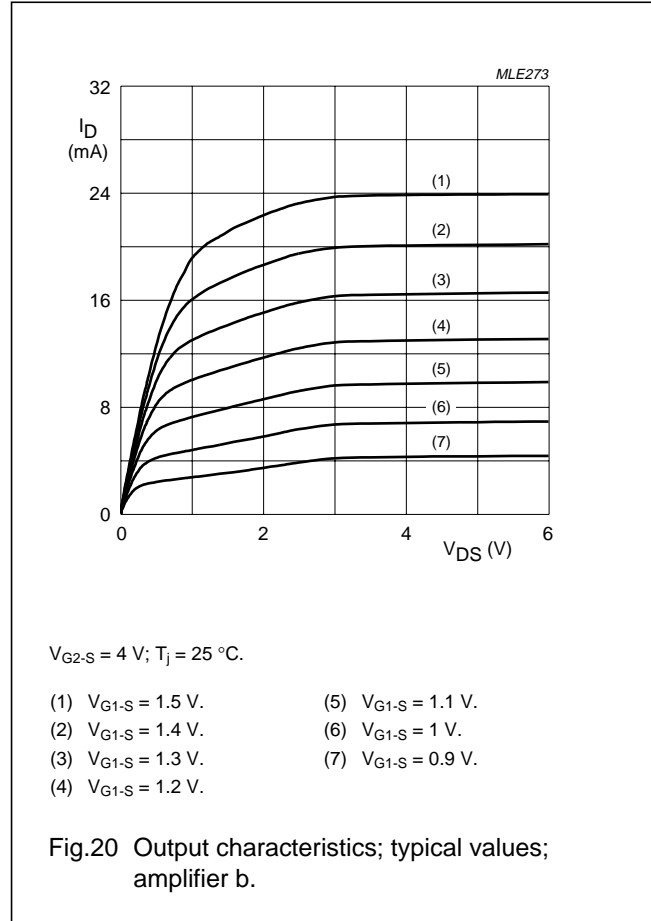
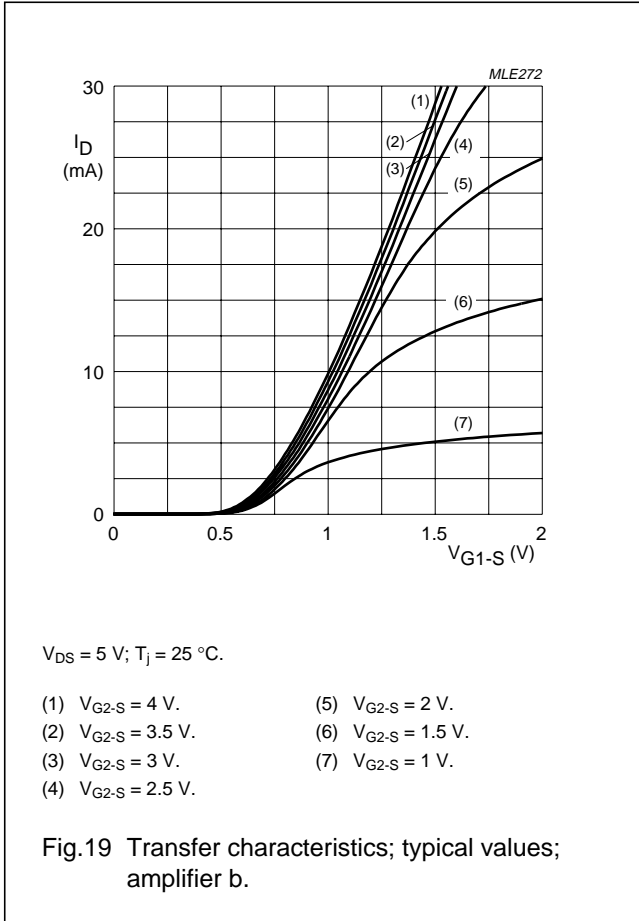
**Notes**

1. Calculated from measured s-parameters.
2. Measured in Fig.35 test circuit.

Dual N-channel dual-gate MOS-FET

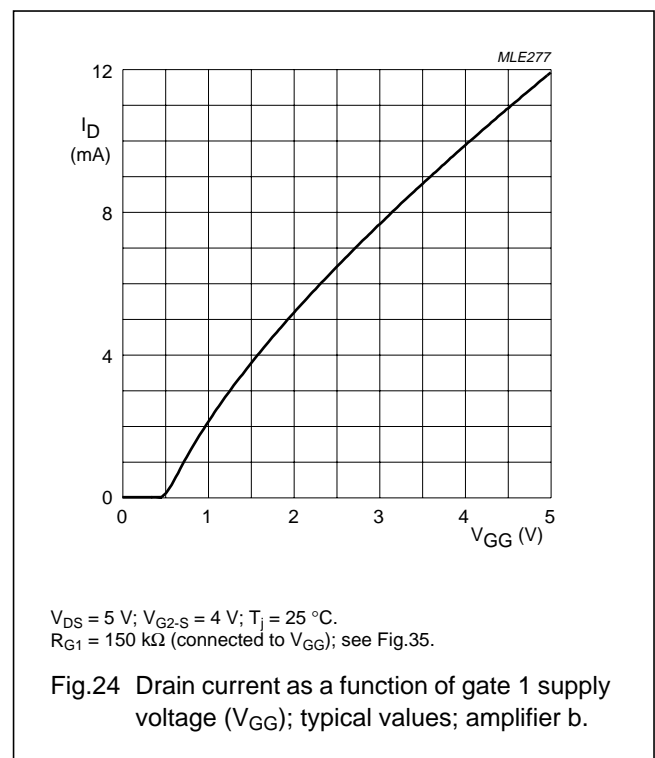
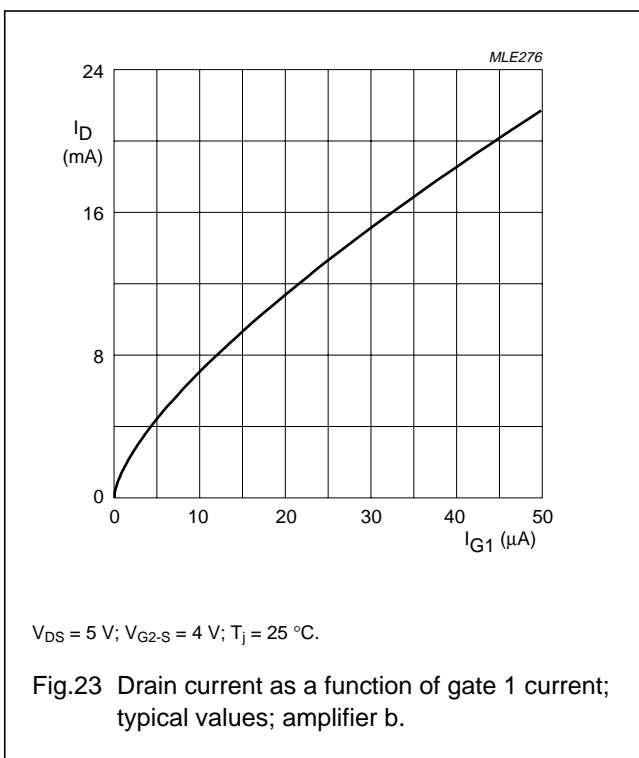
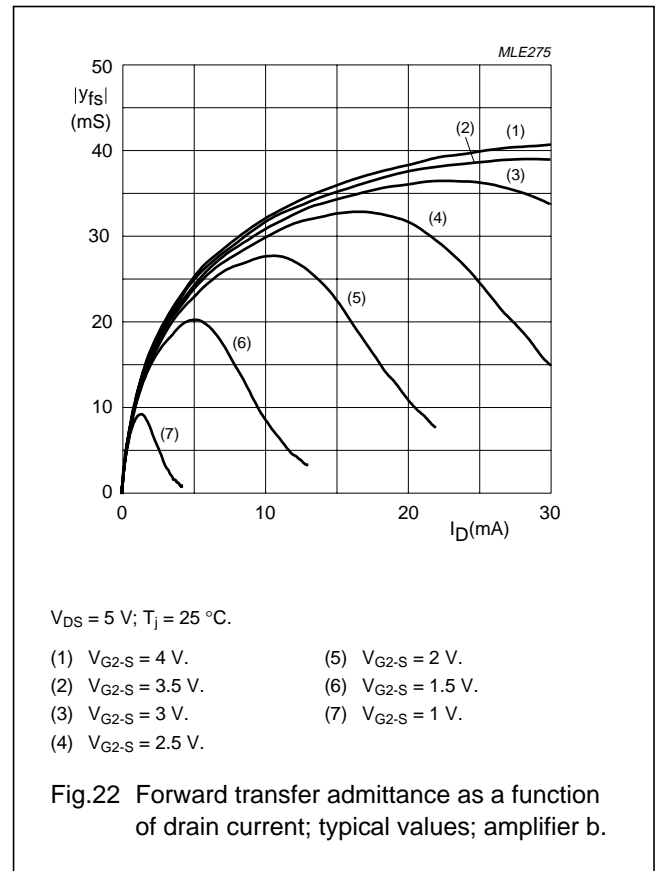
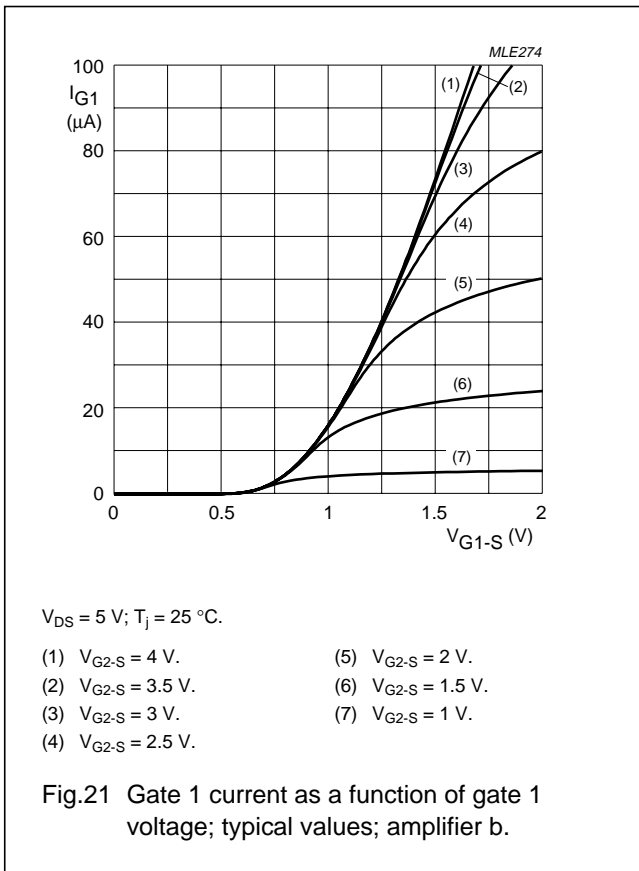
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GRAPHS FOR AMPLIFIER b



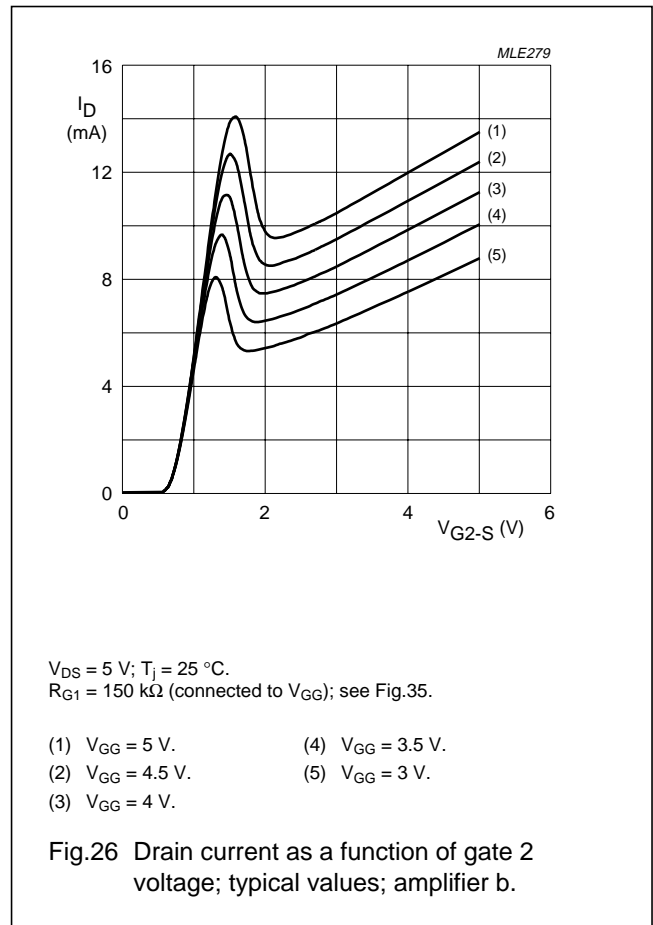
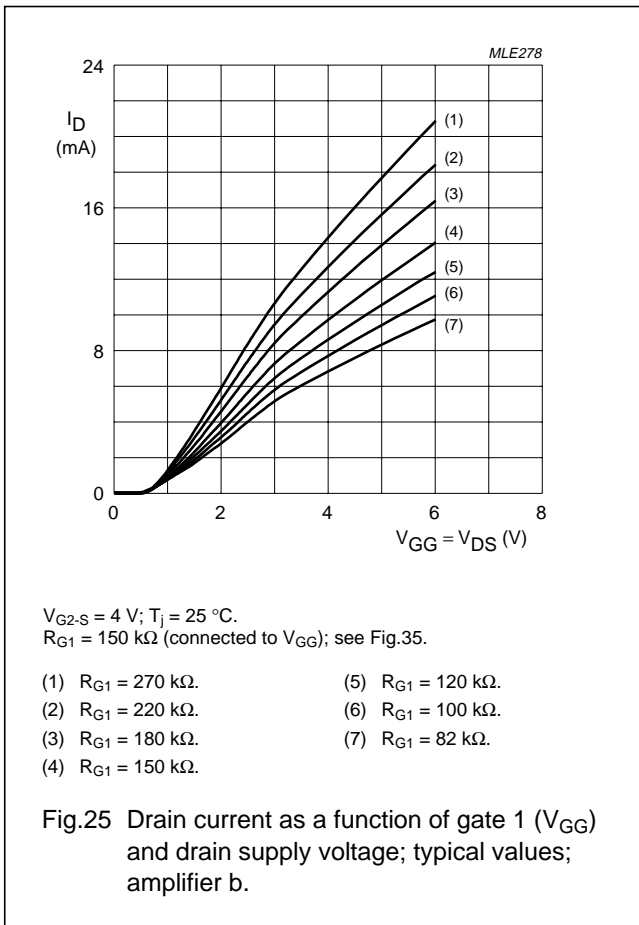
Dual N-channel dual-gate MOS-FET

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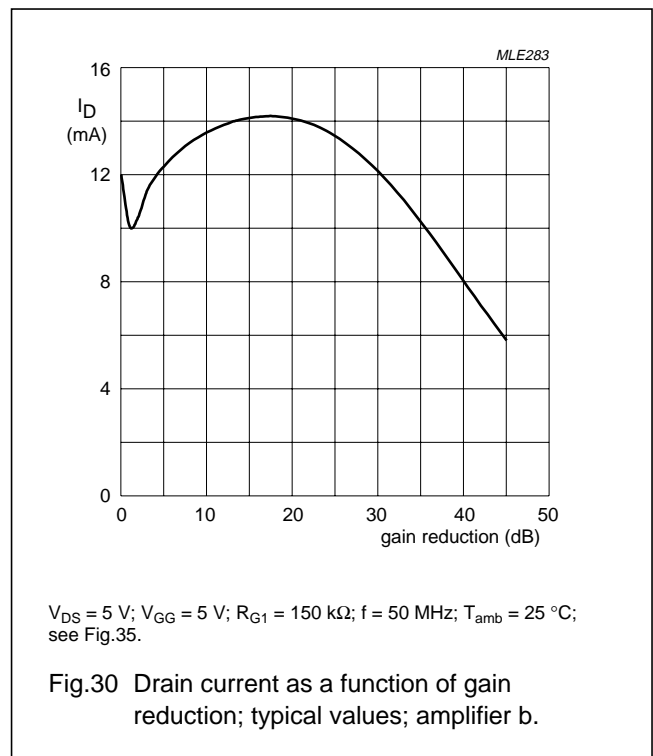
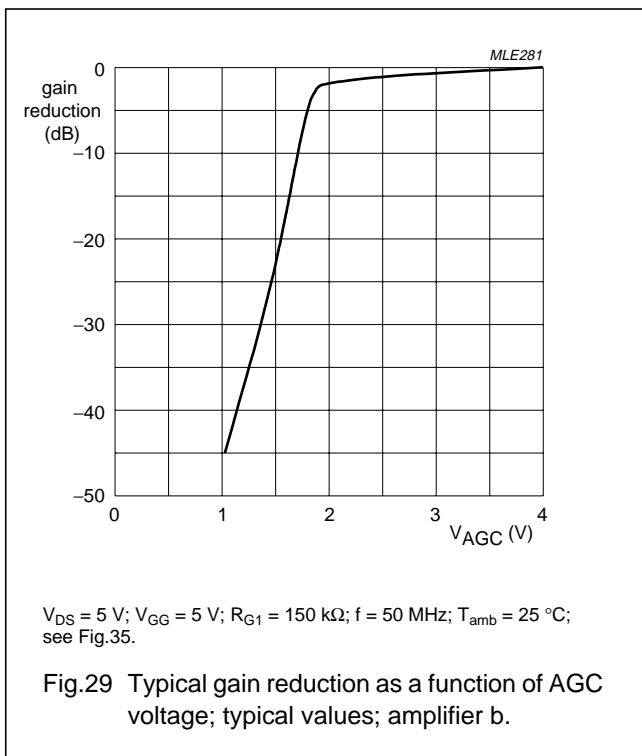
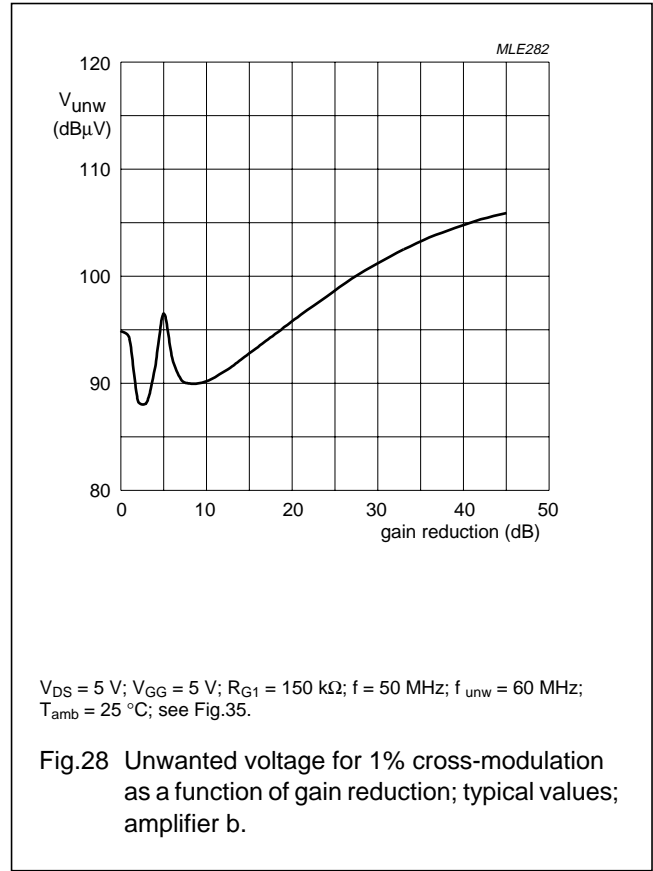
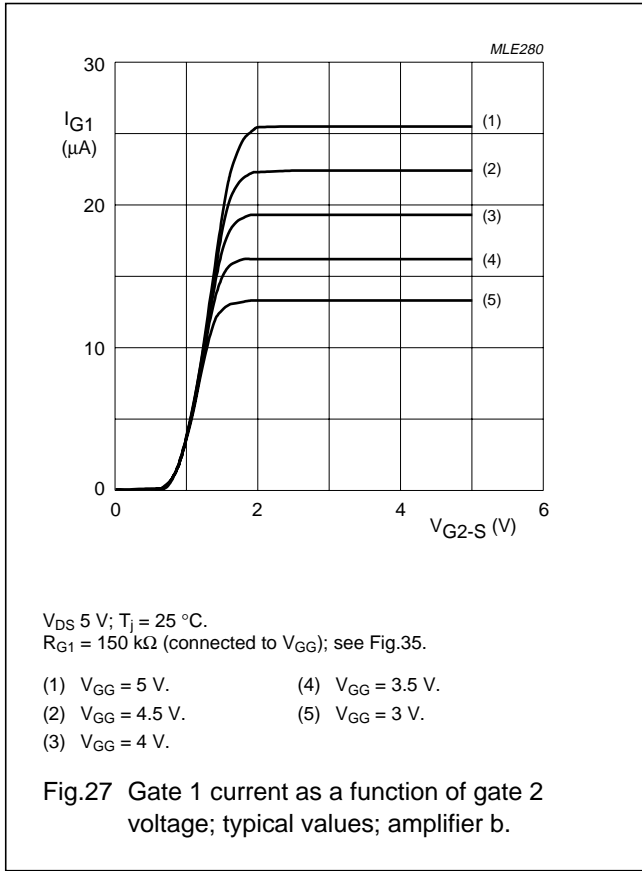
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Dual N-channel dual-gate MOS-FET

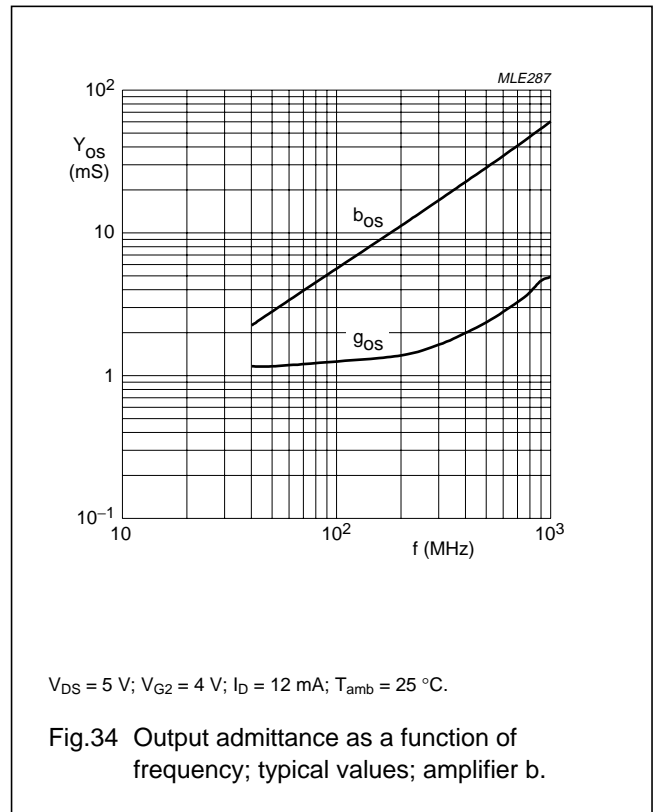
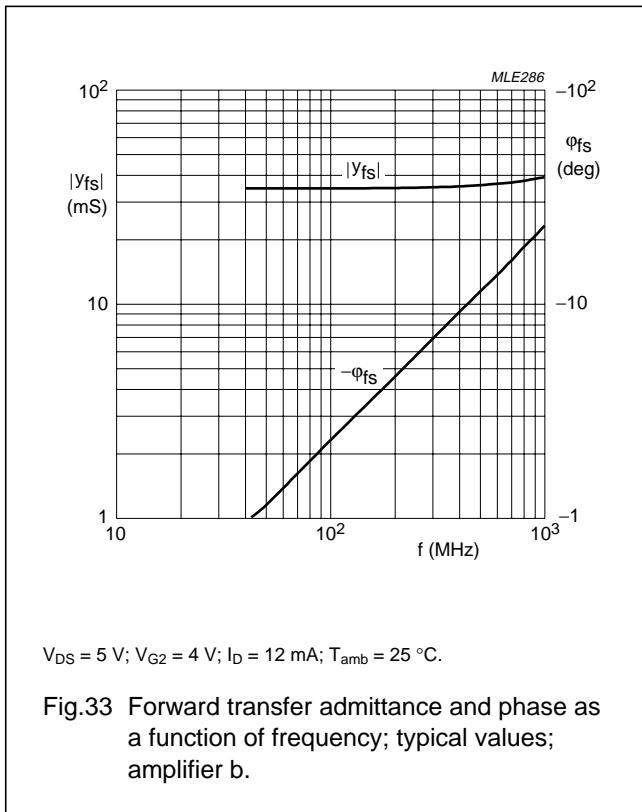
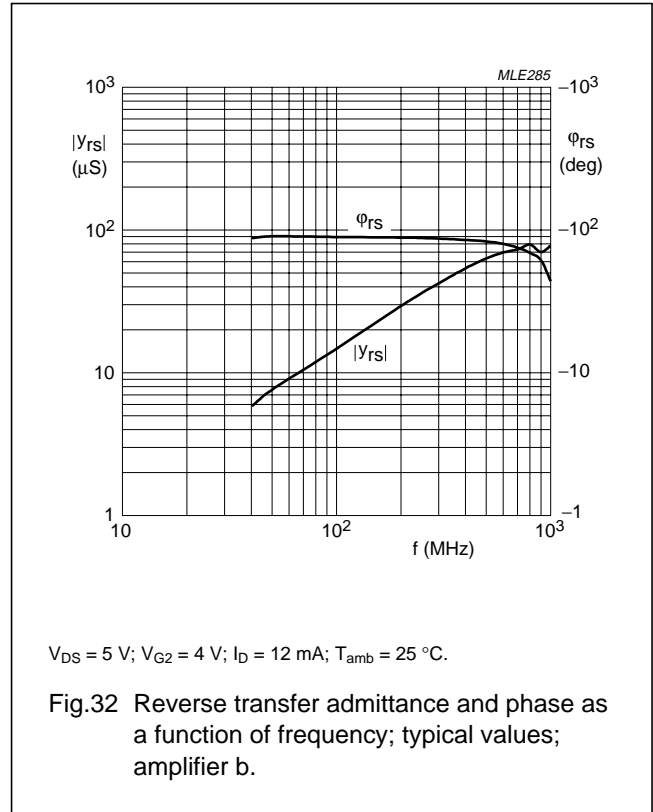
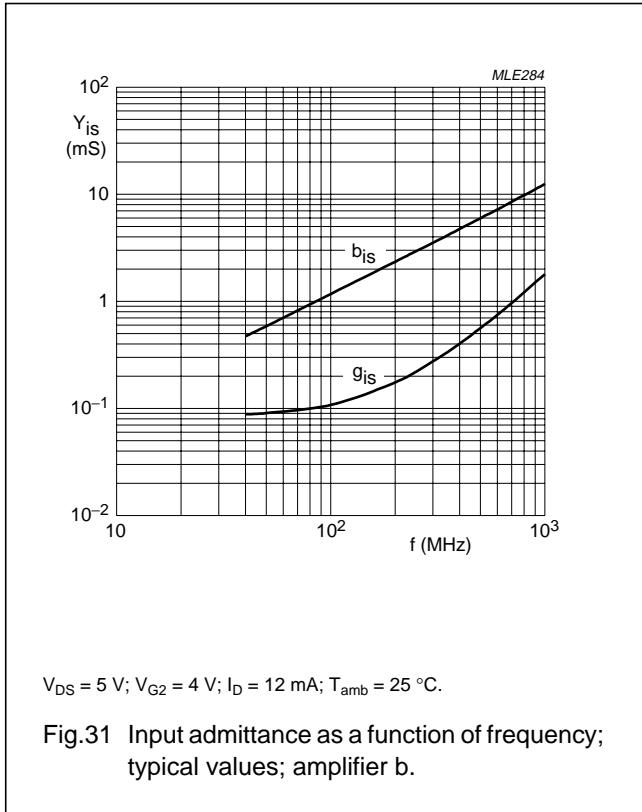
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Dual N-channel dual-gate MOS-FET

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Dual N-channel dual-gate MOS-FET

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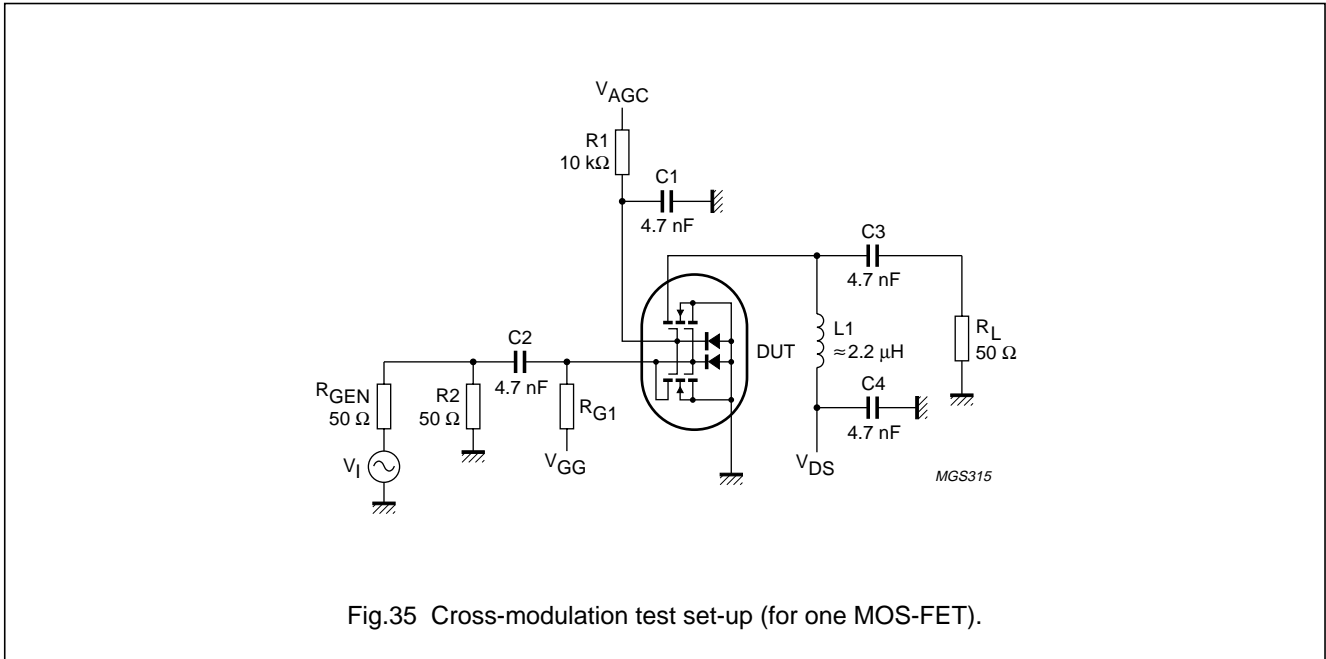


Fig.35 Cross-modulation test set-up (for one MOS-FET).

Amplifier b scattering parameters

$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 12\text{ mA}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$

f (MHz)	S11		S21		S12		S22	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.991	-3.43	3.44	176.33	0.0008	86.54	0.988	-1.69
100	0.989	-6.84	3.43	172.66	0.0015	84.92	0.987	-3.38
200	0.982	-13.61	3.41	165.44	0.0029	80.95	0.985	-6.72
300	0.973	-20.37	3.38	158.20	0.0041	77.63	0.982	-10.08
400	0.961	-27.05	3.34	151.04	0.0051	74.43	0.978	-13.46
500	0.947	-33.68	3.29	144.02	0.0058	71.86	0.973	-16.83
600	0.933	-40.17	3.23	137.12	0.0062	70.28	0.969	-20.25
700	0.919	-46.54	3.16	130.22	0.0063	70.72	0.965	-23.68
800	0.905	-52.86	3.09	123.22	0.0065	72.37	0.960	-27.22
900	0.890	-58.60	3.02	116.84	0.0055	75.91	0.958	-30.57
1000	0.881	-64.34	2.94	110.20	0.0058	89.82	0.958	-34.14

Noise data

$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 12\text{ mA}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$

f (MHz)	F <sub>min</sub> (dB)	Γ <sub>opt</sub>		R <sub>n</sub> (Ω)
		(ratio)	(deg)	
400	1.3	0.648	14.4	28.8
800	1.4	0.604	31.1	27.9

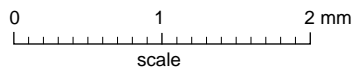
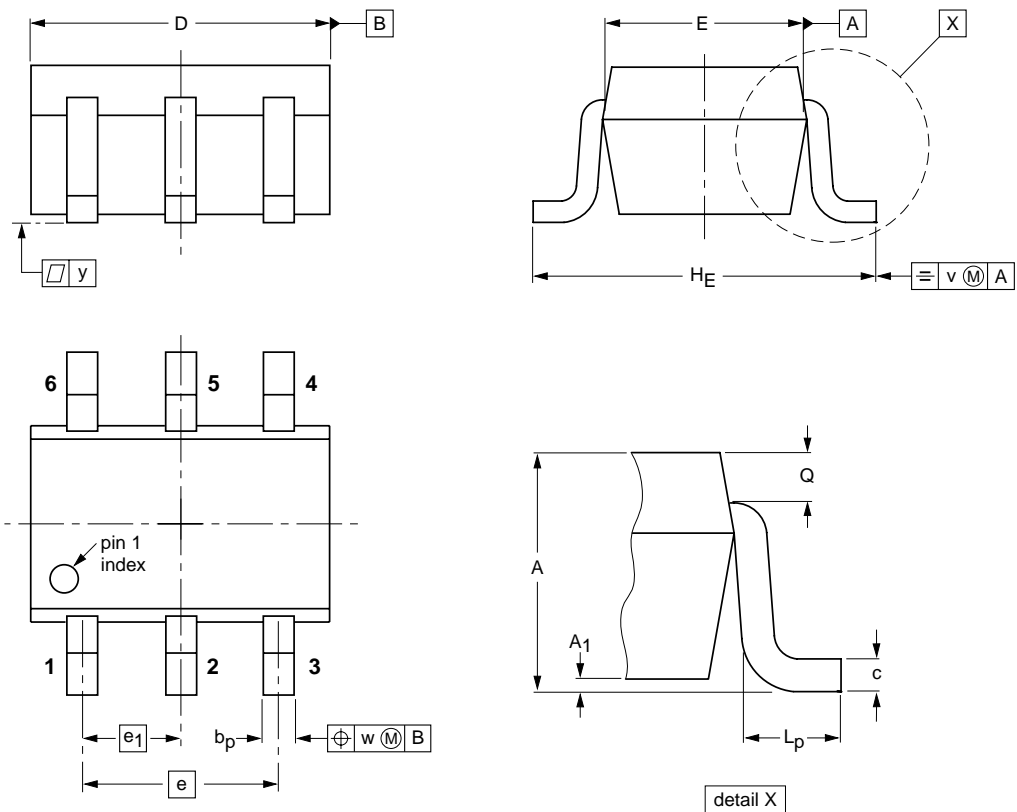
# Dual N-channel dual-gate MOS-FET

BF1206

## PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

## Dual N-channel dual-gate MOS-FET

BF1206

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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